REMARKS

Claims 1-48 are currently pending in the application and all claims stand rejected. Applicants propose herein to amend claims 1, 17, 25, 31, 33, and 37, to cancel claims 28, 29, and 30, and to add new claims 49-63. Applicants respectfully request reconsideration of the amended application in view of the remarks set forth below.

Drawing Correction

Accompanying this response is a Letter to the Official Draftsperson, wherein a change is proposed to FIG. 5. Specifically, reference numeral 300 is being added to FIG. 5, this reference numeral having been inadvertently omitted from the substitute drawings filed with the Preliminary Amendment on May 7, 2001. Reference numeral 300 was included in the informal drawings originally filed with the application.

A red-marked copy of FIG. 5 illustrating the above-described correction, as well as a substitute drawing sheet for FIG. 5, accompany the Letter to the Official Draftsperson. No new matter has been added by way of this amendment to FIG. 5.

Obviousness Rejections Under 35 U.S.C. § 103

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When establishing a prima facie case of obviousness, the Examiner must set forth evidence showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references (or references when combined) must teach or suggest all the claim limitations.
> M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed.

Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

Obviousness Rejection Based on United States Patent 5,675,297 to Gose et al. in View of United States Patent 5,713,030 to Evoy

Claims 1, 9, 17, 34, 37, 38, 39, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 5,675,297 to Gose et al. (hereinafter "the Gose patent") in view of United States Patent 5,713,030 to Evoy (hereinafter "the Evoy patent"). Applicants respectfully traverse this rejection as set forth below.

Claims 1, 9, 17, and 37-40

Claim 1 recites a "thermal management system **located on an integrated circuit die**" including the limitations of a "temperature detection element **formed directly on** an integrated circuit die, the temperature detection element including at least one temperature sensor having an output"; a "power modulation element **formed directly on** the integrated circuit die, the power modulation element to reduce power consumption of the integrated circuit die in response to the output of the at least one temperature sensor"; a "control element **formed directly on** the integrated circuit die, the control element including at least one register to provide an enable/disable bit for the thermal management system"; and a "visibility element **formed directly on** the integrated circuit die, the visibility element to indicate a status of the output of the at least one temperature sensor." Each of claim 9 and amended claim 17 recites similar limitations.

Claim 37, as amended, recites a "method of forming a thermal management system on an integrated circuit die" including the limitations of "forming a temperature detection element **directly on a die**"; "forming a power modulation element **directly on the die**"; "forming a control element **directly on the die**"; and "forming a visibility element **directly on the die**."

The Examiner states that the Gose patent teaches "a thermo management system with power modulation element, control element, [and] visibility element to indicate status of the output." Office Action, at page 2. The Examiner further states "Gose *does*

not disclose the temperature detection element formed on an microprocessor integrated circuit die" but that "Evoy disclose the computer system with temperature detection element *formed on* an microprocessor integrated circuit die." Office Action, at page 2 (emphasis added).

The Gose patent discloses a conditional protection circuit 10 having a pulse-width modulation (PWM) circuit 12, a thermal shutdown circuit 20, and a TSD (thermal shutdown) detection circuit 16. Column 1, Lines 14-27; FIG. 1. The Evoy patent is directed to a thermal management device and method for a microprocessor. Column 1, Lines 5-7. However, in contrast to the Examiner's assertion, the Evoy patent does not teach a temperature detection element "formed directly on" an integrated circuit die, as claimed in each of claims 1, 9, 17, and 37. As specifically stated in the Evoy patent, the thermal management system is provided on a "**separately packaged** integrated circuit clock chip . . . coupled to the processor for controlling the frequency of operation of the processor." Column 3, Lines 14-25; Column 3, Lines 60-67 through Column 4, Lines 1-5; Column 4, Lines 12-23.

The cited prior art, in general, does not teach or suggest a thermal management system for an integrated circuit die, wherein all elements (e.g., temperature detection element, power modulation element, control element, and visibility element) of the thermal management system are formed directly on the die. Accordingly, the Gose and Evoy patents, either individually or in combination, do not teach a thermal management system wherein all elements thereof are "formed directly on" an integrated circuit die, as claimed in each of claims 1, 9, 17, and 37. Claims 1, 17, and 37 were amended herein to clarify that the claimed invention is directed to a thermal management system located and formed directly on an integrated circuit die.

In summary, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest at least the limitations of a thermal management system "located on" and "formed directly on" a die. Therefore, a prima facie case of obviousness can not be made out with respect to claims 1, 9, 17, and 37 based upon the Gose and/or Evoy patents, respectively, and each of claims 1, 9, 17, and 37 is nonobvious in view of the Gose and Evoy patents.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 38-40 are allowable as depending from nonobvious, independent claim 37.

Claim 34

Claim 34 is directed to an "apparatus" and recites, in part, a "visibility element . . . including a register to indicate the status of the output of the at least one temperature sensor; a register providing a sticky bit; a counter to count a number of lost clock cycles resulting from operation of the apparatus; and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state." The Gose and Evoy patent, either individually or in combination, do not teach a visibility element that includes the recited limitations (i.e., a register to indicate status at output of temperature sensor, a register providing a sticky bit, a counter to count lost clock cycles, and circuitry to generate an interrupt), and the Examiner has failed to set forth any specific teaching or suggestion from the Gose and Evoy patents to the contrary.

As the Gose and Evoy patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations of claim 34, a prima facie case of obviousness has not been set forth with respect to claim 34. Thus, claim 34 is nonobvious in view of the Gose and Evoy patents.

Obviousness Rejection Based on United States Patent 5,675,297 to Gose et al. in View of United States Patent 5,713,030 to Evoy and Further in View of United States Patent 5,838,578 to Pippin

Claims 2, 6, 7, 8, 10, 14, 15, 16, 18, 22-33, 35, and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Gose patent in view of the Evoy patent and further in view of United States Patent 5,838,578 to Pippin (hereinafter "the Pippin patent"). Claims 28, 29, and 30 were canceled herein. Applicants respectfully traverse this rejection as set forth below.

Claims 2, 6-8, 10, 14-16, 18, and 22-24

The respective disclosures of the Gose and Evoy patents are summarized above. The Pippin patent discloses a programmable thermal sensor implemented in an integrated circuit. Column 2, Lines 7-8. As noted above, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest a thermal management system wherein all elements of the thermal management system are formed directly on an integrated circuit die. The Pippin patent also fails to teach or suggest a thermal management system wherein all elements of the thermal management system are formed directly on a die. Accordingly, the Gose, Evoy, and Pippin patents, either individually or in combination, fail to teach or suggest the claimed thermal management system located and formed directly on a die. Thus, independent claims 1, 9, and 17 are nonobvious in view of the Gose, Evoy, and Pippin patents.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 2 and 6-8 are allowable as depending from nonobvious, independent claim 1. Similarly, claims 10 and 14-16 are allowable as depending from nonobvious, independent claim 9, whereas claims 18 and 22-24 are allowable as depending from nonobvious, independent claim 17.

Also, as will be discussed below, the Pippin patent does not teach or suggest the limitations of claims 6, 14, and 22, respectively.

Claims 35 and 36

The respective disclosures of the Gose, Evoy, and Pippin patents are summarized above. As noted above, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest the "visibility element," as claimed in independent claim 34 (including the limitations of a register to indicate the status at an output of a temperature sensor, a register providing a sticky bit, a counter to count lost clock cycles, and circuitry to generate an interrupt). The Pippin patent also fails to teach a visibility element including at least the limitations of a register to indicate the status at an output of a temperature sensor, a register providing a sticky bit, and a counter to count lost clock cycles, and the Examiner has failed to set forth any specific teaching or suggestion from

the Pippin patent to the contrary (The Examiner expressly states – Office Action, at page 5 – that Pippin fails to disclose a sticky bit). Accordingly, the Gose, Evoy, and Pippin patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations of independent claim 34 and, therefore, claim 34 is nonobvious in view of the Gose, Evoy, and Pippin patents.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, claims 35 and 36 are allowable as depending from nonobvious, independent claim 34.

Claims 25-33

The Gose, Evoy, and Pippin patents, either individually or in combination, fail to teach or suggest all limitations of dependent claims 28, 29, and 30. Claim 25 was amended herein to include limitations similar to those recited in dependent claim 28. Therefore, because the cited prior art, either individually or in combination, fails to teach or suggest all limitations of independent claim 25, this claim is nonobvious in view of the Gose, Evoy, and Pippin patents.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 26, 27, 31, 32, 33, and new claim 49 are allowable as depending from nonobvious, independent claim 25.

It should be noted that new claim 50 includes limitations similar to those recited in canceled claim 29 (including those recited in the base claim), whereas new claim 57 includes limitations similar to those recited in canceled claim 30 (including those recited in the base claim). Dependent claims 28, 29, and 30 were canceled herein. Therefore, new claims 50-63, respectively, are allowable over the cited prior art.

Obviousness Rejection Based on United States Patent 5,675,297 to Gose et al. in View of United States Patent 5,713,030 to Evoy and Further in View of United States Patents 6,137,329 to Kardash and 6,336,593 to Bhatnagar

Claims 3-5, 11-13, and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Gose patent in view of the Evoy patent and further in view of United States Patent 6,137,329 to Kardash (hereinafter "the Kardash patent") and United States Patent 6,336,593 to Bhatnagar (hereinafter "the Bhatnagar patent"). Applicants respectfully traverse this rejection as set forth below.

The respective teachings of the Evoy and Gose patents are summarized above. The Kardash patent discloses a controller for controlling the voltage slew-rate of an inductive load connected to a field effect transistor and a controller for driving an inductive load. Column 2, Lines 14-54. The Bhatnagar patent discloses a multi-point compact electronic control unit having an electronic digital thermostat. Column 2, Lines 59-68 through Column 3, Lines 1-27.

As noted above, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest a thermal management system wherein all elements of the thermal management system are formed directly on an integrated circuit die. The Kardash and Bhatnagar patents, respectively, also fail to teach or suggest a thermal management system wherein all elements of the thermal management system are formed directly on a die. Accordingly, the Gose, Evoy, Kardash, and Bhatnagar patents, either individually or in combination, fail to teach or suggest the claimed thermal management system located and formed directly on a die. Thus, independent claims 1, 9, and 17 are nonobvious in view of the Gose, Evoy, Kardash, and Bhatnagar patents.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 3-5, 11-13, and 19-21 are allowable as depending from nonobvious, independent claims 1, 9, and 17, respectively.

Obviousness Rejection Based on United States Patent 5,838,578 to Pippin in View of United States Patent 6,101,516 to Wolrich et al.

Claims 41-43 and 45-47 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Pippin patent in view of United States Patent 6,101,516 to Wolrich et al. (hereinafter "the Wolrich patent"). Applicants respectfully traverse this rejection as set forth below.

Claims 41-43

Claim 41 recites an "apparatus" including the limitations of a "first register **to provide an enable/disable bit** for a thermal management system on an integrated circuit die"; a "second register **to selectively disengage a specified portion** of the thermal management system"; a "third register **to enable the thermal management system in response to an external event**"; a "fourth register **to force the thermal management system active while overriding** a disable bit provided by the first register"; and a "fifth register **to allow external software and hardware to enable** the thermal management system."

The Examiner states that:

> "Pippin disclose and suggested apparatus for thermo management system with register to enable and disable bit, to disengage a specific portion of the thermo management system, with external event, can override (fig. 7-11), allow external software and hardware to enable the for thermo management system (fig. 11) . . . ." Office Action, at page 4.

The Applicants believe, respectfully, that the Examiner's characterization of the Pippin patent is incorrect. As set forth above, the Pippin patent discloses a programmable thermal sensor implemented in an integrated circuit. Column 2, Lines 7-8. The only register included in this programmable thermal sensor, as shown and described in the Pippin patent, is an internal register 735, 920 (see FIGS. 7 and 9). This internal register 735, 920 stores a threshold temperature value (or values) for the thermal sensor. Column 10, Lines 51-63; Column 12, Lines 22-24. The disclosed internal register 735, 930 does not, however, provide an enable/disable bit, selectively disengage a specified portion of a

thermal management system, enable a thermal management system in response to an external event, force a thermal management system active while overriding a disable bit, or allow external software and hardware to enable a thermal management system, all as recited in independent claim 41. The Examiner has not identified any specific teaching in the Pippin patent to the contrary.

The Wolrich patent discloses a method and apparatus for predicting a normalization shift during floating point add-subtract operations. Column 2, Lines 29-67. The Wolrich patent also fails to disclose any of the claimed registers.

In sum, the Pippin and Wolrich patents, either individually or in combination, fail to disclose the limitations of a "first register **to provide an enable/disable bit** for a thermal management system on an integrated circuit die"; a "second register **to selectively disengage a specified portion** of the thermal management system"; a "third register **to enable the thermal management system in response to an external event**"; a "fourth register **to force the thermal management system active while overriding** a disable bit provided by the first register"; and a "fifth register **to allow external software and hardware to enable** the thermal management system." Thus, a prima facie case of obviousness has not been made out with respect to independent claim 41, and claim 41 is nonobvious in view of the Pippin and Wolrich patents.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 42 and 43 are allowable as depending from nonobvious, independent claim 41.

Claims 45-47

Claim 45 recites an "apparatus" including the limitations of a "register to indicate a status of an output of a temperature sensor associated with a thermal management system on an integrated circuit die"; "another register to provide a **sticky bit**"; a "**counter to count a number of lost clock cycles** resulting from operation of the thermal management system"; and "circuitry to generate an interrupt when the temperature sensor output transitions to a different state."

The respective teachings of the Pippin and Wolrich patents are summarized above. The Examiner states that the Pippin patent discloses a "counter to count number of clock" cycles. Office Action, at page 5. The Applicants respectfully disagree that the Pippin patent discloses the claimed "counter to count a number of lost clock cycles resulting from operation of the thermal management system."

The only counter shown and described in the Pippin patent is the counter 950 illustrated in FIG. 9. However, as stated in the Pippin patent, the "counter 950 is configured as a frequency divider such that a clock frequency, from the external clock 945, is input" and the "counter 950 generates a new clock frequency based on the counter value." Column 12, Lines 35-40. Thus, according to the express description of the counter 950 provided in the written specification of the Pippin patent, the counter 950 does not count a number of lost clock cycles. The Wolrich patent also fails to disclose any counter to count a number of lost clock cycles resulting from operation of a thermal management system.

Thus, the Pippin and Wolrich patents, either individually or in combination, fail to teach or suggest at least the limitation of a counter to count a number of lost clock cycles, as claimed in independent claim 45. Accordingly, claim 45 is nonobvious in view of the Pippin and Wolrich patents.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 46 and 47 are allowable as depending from nonobvious, independent claim 45.

Obviousness Rejection Based on United States Patent 5,838,578 to Pippin in View of United States Patent 6,101,516 to Wolrich et al. and Further in View of United States Patent 5,675,297 to Gose et al.

Claims 44 and 48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Pippin patent in view of the Wolrich patent and further in view of the Gose patent. Applicants respectfully traverse this rejection as set forth below.

Claim 44

The respective teachings of the Pippin, Wolrich, and Gose patents are summarized above.

As noted above the Pippin and Wolrich patents, either individually or in combination, fail to disclose the limitations of a "first register to provide an enable/disable bit for a thermal management system on an integrated circuit die"; a "second register to selectively disengage a specified portion of the thermal management system"; a "third register to enable the thermal management system in response to an external event"; a "fourth register to force the thermal management system active while overriding a disable bit provided by the first register"; and a "fifth register to allow external software and hardware to enable the thermal management system." The Gose patent also fails to teach or suggest at least the limitations of a "second register to selectively disengage a specified portion of the thermal management system"; a "third register to enable the thermal management system in response to an external event"; a "fourth register to force the thermal management system active while overriding a disable bit provided by the first register"; and a "fifth register to allow external software and hardware to enable the thermal management system."

In sum, the Pippin, Wolrich, and Gose patents, either individually or in combination, fail to teach or suggest all limitations of independent claim 41, and a prima facie case of obviousness can not be set forth with respect to claim 41 based upon the cited prior art. Thus, claim 41 is nonobvious in view of the Pippin, Wolrich, and Gose patents.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claim 44 is allowable as depending from nonobvious, independent claim 41.

Claim 48

The respective teachings of the Pippin, Wolrich, and Gose patents are summarized above.

As noted above the Pippin and Wolrich patents, either individually or in combination, fail to teach or suggest at least the limitation of a counter to count a number of lost clock cycles. The Gose patent also fails to teach or suggest this limitation. Thus, the Pippin, Wolrich, and Gose patents, either individually or in combination, fail to teach or suggest all limitations of independent claim 45, and a prima facie case of obviousness can not be set forth with respect to claim 45 based upon the cited prior art. Accordingly, claim 45 is nonobvious in view of the Pippin, Wolrich, and Gose patents.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claim 48 is allowable as depending from nonobvious, independent claim 45.

CONCLUSION

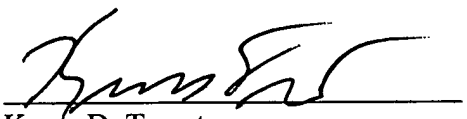
Applicants submit that claims 1-27 and 31-63 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, L.L.P.

Date: June 20, 2002



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MARKED UP VERSION OF THE AMENDED CLAIMS

1. (Twice Amended) A thermal management system <u>located on an integrated circuit die</u> comprising:

a temperature detection element formed directly on an integrated circuit die, the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on the integrated circuit die, the power modulation element to reduce power consumption of the integrated circuit die in response to the output of the at least one temperature sensor;

a control element formed directly on the integrated circuit die, the control element including at least one register to provide an enable/disable bit for the thermal management system; and

a visibility element formed directly on the integrated circuit die, the visibility element to indicate a status of the output of the at least one temperature sensor.

2. (Amended) The system of claim 1, the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of the integrated circuit die; and

a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage.

3. (Amended) The system of claim 2, further comprising a pulse dampener coupled to the first signal line, the pulse dampener to at least partially remove electrical noise from the reference voltage.

4. (Amended) The system of claim 2, further comprising an analog filter coupled to the second signal line and the first signal line, the analog filter to detect voltage spikes present in the reference voltage and to add substantially identical voltage spikes to the programmable voltage.

5. (Amended) The system of claim 2, further comprising a digital filter coupled to an output of the comparator, the digital filter including an up-down counter to count clock pulses, the up-down counter to increment once for each clock pulse detected when the comparator output is at a first state and to decrement once for each clock pulse detected when the comparator output is at a second state.

6. (Amended) The system of claim 1, the control element further including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system.

7. (Amended) The system of claim 1, the visibility element including at least one of a register to indicate the status of the temperature sensor output, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

8. (Amended) The system of claim 1, the power modulation element to reduce the power consumption of the integrated circuit die by performing at least one of lowering a supply voltage to the integrated circuit die, lowering a frequency of a clock signal provided by internal clock circuitry on the integrated circuit die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the integrated circuit die, limiting instructions sent to at least one of the plurality of functional units on the integrated circuit die, and changing a behavior of at least one of the plurality of functional units on the integrated circuit die.

9. (Amended) A microprocessor comprising:
a die having a plurality of functional units formed thereon;
internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and
a thermal management system formed directly on the die, the thermal management system including
a temperature detection element including at least one temperature sensor having an output;
a power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor;
a control element including at least one register to provide an enable/disable bit for the thermal management system; and
a visibility element to indicate a status of the output of the at least one temperature sensor.

10. (Amended) The microprocessor of claim 9, the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of the die; and

a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage.

11. (Amended) The microprocessor of claim 10, further comprising a pulse dampener coupled to the first signal line, the pulse dampener to at least partially remove electrical noise from the reference voltage.

12. (Amended) The microprocessor of claim 10, further comprising an analog filter coupled to the second signal line and the first signal line, the analog filter to detect voltage spikes present in the reference voltage and to add substantially identical voltage spikes to the programmable voltage.

13. (Amended) The microprocessor of claim 10, further comprising a digital filter coupled to an output of the comparator, the digital filter including an up-down counter to count clock pulses, the up-down counter to increment once for each clock pulse detected when the comparator output is at a first state and to decrement once for each clock pulse detected when the comparator output is at a second state.

14. (Amended) The microprocessor of claim 9, the control element further including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system.

15. (Amended) The microprocessor of claim 9, the visibility element including at least one of a register to indicate the status of the temperature sensor output, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

16. (Amended) The microprocessor of claim 9, the power modulation element to reduce the power consumption of the at least one functional unit by performing at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by the internal clock circuitry, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of the plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

17. (Twice Amended) A computer system comprising:

at least one memory device coupled to a bus; and

at least one microprocessor coupled to the bus [and the at least one memory device], the at least one microprocessor including

a die having a plurality of functional units formed thereon;

internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and

a thermal management system located on the die, the thermal management system including

a temperature detection element formed directly on the die, the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on the die, the power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor;

a control element formed directly on the die, the control element including at least one register to provide an enable/disable bit; and

a visibility element formed directly on the die, the visibility element to indicate a status of the output of the at least one temperature sensor[, the temperature detection, power modulation, control, and visibility elements comprising a thermal management system for the die].

18. (Amended) The computer system of claim 17, the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of the die; and

a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage.

19. (Amended) The computer system of claim 18, further comprising a pulse dampener coupled to the first signal line, the pulse dampener to at least partially remove electrical noise from the reference voltage.

20. (Amended) The computer system of claim 18, further comprising an analog filter coupled to the second signal line and the first signal line, the analog filter to detect voltage spikes present in the reference voltage and to add substantially identical voltage spikes to the programmable voltage.

21. (Amended) The computer system of claim 18, further comprising a digital filter coupled to an output of the comparator, the digital filter including an up-down counter to count clock pulses, the up-down counter to increment once for each clock pulse detected when the comparator output is at a first state and to decrement once for each clock pulse detected when the comparator output is at a second state.

22. (Amended) The computer system of claim 17, the control element further including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system.

23. (Amended) The computer system of claim 17, the visibility element including at least one of a register to indicate the status of the temperature sensor output, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

24. (Amended) The computer system of claim 17, the power modulation element to reduce the power consumption of the at least one functional unit by performing at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by the internal clock circuitry, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of the plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

25. (Twice Amended) A method comprising:
providing an enable bit to a register to activate a thermal management system of a die;
measuring a temperature on the die with a sensor of the thermal management system;
providing a first state at an output of the sensor when the temperature is below a trip point;
providing a second state at the sensor output when the temperature equals or exceeds the trip point;
in response to the sensor output having the second state, engaging a power reduction mechanism for a specified time period to reduce power consumption of the die [in response to the sensor output]; [and
providing an indication of a status of the sensor output to an external device]
polling the sensor output after expiration of the specified time period;
engaging the power reduction mechanism for at least another one of the specified time periods if the sensor output exhibits the second state; and
halting the power reduction mechanism when the sensor output exhibits the first state.

26. (Amended) The method of claim 25, further comprising engaging the power reduction mechanism to perform at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by internal clock circuitry on the die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

27. (Amended) The method of claim 25, further comprising providing an enable bit to the register from an external operating system.

28. (Canceled) The method of claim 25, further comprising:
engaging the power reduction mechanism for a specified time period;
polling the sensor output after expiration of the specified time period;
engaging the power reduction mechanism for at least another one of the specified time periods when the sensor output exhibits the second state; and
halting the power reduction mechanism when the sensor output exhibits the first state.

29. (Canceled) The method of claim 25, further comprising:
engaging the power reduction mechanism for a specified time period;
continuously polling the sensor output after expiration of the specified time period; and
halting the power reduction mechanism when the sensor output exhibits the first state.

30. (Canceled) The method of claim 25, further comprising:
providing the first state at the sensor output when the temperature is below an untrip point, the untrip point less than the trip point; and
halting the power reduction mechanism in response to the first state.

31. (Twice Amended) The method of claim 25, further comprising:
[coupling an up-down counter to the sensor output;]
incrementing [the] an up-down counter coupled with the sensor output once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the first state; and
decrementing the up-down counter once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the second state.

32. (Amended) The method of claim 25, further comprising:
defining a plurality of trip temperatures, a highest of the plurality of trip temperatures corresponding to the trip point;
assigning a plurality of duty cycle values to the plurality of trip temperatures, one duty cycle value of the plurality of duty cycle values corresponding to at least one of the plurality of trip temperatures; and
providing a clock signal from the internal clock circuitry exhibiting the one duty cycle value in response to the temperature substantially equaling that at least one corresponding trip temperature.

33. (Twice Amended) The method of claim 25, further comprising counting a number of lost clock cycles [eliminated from an output of the internal clock circuitry] resulting from engagement of the power reduction mechanism.

34. (Amended) An apparatus comprising:
a temperature detection element, the temperature detection element including at least one temperature sensor having an output;
a power modulation element, the power modulation element to reduce power consumption of an integrated circuit die in response to the output of the at least one temperature sensor;
a visibility element, the visibility element to indicate a status of the output of the at least one temperature sensor, the visibility element including
a register to indicate the status of the output of the at least one temperature sensor;
a register providing a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of the apparatus; and
circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

35. (Amended) The apparatus of claim 34, further including a control element, the control element comprising:
a register to provide an enable/disable bit for the apparatus;
a register to selectively disengage a specified portion of the apparatus;
a register to enable the apparatus in response to an occurrence of an external event;
a register to force the apparatus active while overriding a disable bit provided at the enable/disable bit; and
a register to allow external software and hardware to enable the apparatus.

36. (Amended) The system of claim 34, the power modulation element to reduce the power consumption of the integrated circuit die by performing at least one of lowering a supply voltage to the integrated circuit die, lowering a frequency of a clock signal provided by internal clock circuitry on the integrated circuit die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the integrated circuit die, limiting instructions sent to at least one of the plurality of functional units on the integrated circuit die, and changing a behavior of at least one of the plurality of functional units on the integrated circuit die.

37. (Amended) A method <u>of forming a thermal management system on an integrated circuit die</u> comprising:
forming a temperature detection element directly on a die;
forming a power modulation element directly on the die;
forming a control element directly on the die; and
forming a visibility element directly on the die.

38. The method of claim 37, further comprising calibrating a temperature sensor associated with the temperature detection element.

39. The method of claim 37, further comprising forming at least one functional unit on the die.

40. The method of claim 39, further comprising forming circuitry on the die common to the at least one functional unit and at least one of the temperature detection element, power modulation element, control element, and visibility element.

41. An apparatus comprising:
a first register to provide an enable/disable bit for a thermal management system on an integrated circuit die;
a second register to selectively disengage a specified portion of the thermal management system;
a third register to enable the thermal management system in response to an external event;
a fourth register to force the thermal management system active while overriding a disable bit provided by the first register; and
a fifth register to allow external software and hardware to enable the thermal management system.

42. The apparatus of claim 41, further comprising a visibility element to indicate a status of an output of a temperature sensor associated with the thermal management system.

43. The apparatus of claim 42, the visibility element comprising:
a register to indicate the status of the temperature sensor output;
another register to provide a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of the thermal management system; and
circuitry to generate an interrupt when the temperature sensor output transitions to a different state.

44. The apparatus of claim 42, further comprising a power modulation element to reduce power consumption of the integrated circuit die in response to the temperature sensor output.

45. An apparatus comprising:
a register to indicate a status of an output of a temperature sensor associated with a thermal management system on an integrated circuit die;
another register to provide a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of the thermal management system; and
circuitry to generate an interrupt when the temperature sensor output transitions to a different state.

46. The apparatus of claim 45, further comprising a control element including a first register to provide an enable/disable bit for the thermal management system.

47. The apparatus of claim 46, the control element further comprising:
a second register to selectively disengage a specified portion of the thermal management system;
a third register to enable the thermal management system in response to an external event;
a fourth register to force the thermal management system active while overriding a disable bit provided by the first register; and
a fifth register to allow external software and hardware to enable the thermal management system.

48. The apparatus of claim 46, further comprising a power modulation element to reduce power consumption of the integrated circuit die in response to the temperature sensor output.

49. (New) The method of claim 25, further comprising providing an indication of a status of the sensor output to an external device.

50. (New) A method comprising:
activating a thermal management system of a die;
measuring a temperature on the die with a sensor of the thermal management system;
providing a first state at an output of the sensor when the temperature is below a trip point;
providing a second state at the sensor output when the temperature equals or exceeds the trip point;
engaging a power reduction mechanism for a specified time period in response to the sensor output having the second state;
polling the sensor output after expiration of the specified time period; and
halting the power reduction mechanism when the sensor output exhibits the first state.

51. (New) The method of claim 50, further comprising engaging the power reduction mechanism to perform at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by internal clock circuitry on the die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

52. (New) The method of claim 50, further comprising providing an enable bit to a register from an external operating system to activate the thermal management system.

53. (New) The method of claim 50, further comprising:
incrementing an up-down counter coupled with the sensor output once for every clock pulse of a clock signal provided by internal clock circuitry on the die when the sensor output exhibits the first state; and
decrementing the up-down counter once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the second state.

54. (New) The method of claim 50, further comprising:
defining a plurality of trip temperatures, a highest of the plurality of trip temperatures corresponding to the trip point;
assigning a plurality of duty cycle values to the plurality of trip temperatures, one duty cycle value of the plurality of duty cycle values corresponding to at least one of the plurality of trip temperatures; and
providing a clock signal from internal clock circuitry on the die, the clock signal exhibiting the one duty cycle value in response to the temperature substantially equaling the at least one corresponding trip temperature.

55. (New) The method of claim 50, further comprising counting a number of lost clock cycles resulting from engagement of the power reduction mechanism.

56. (New) The method of claim 50, further comprising providing an indication of a status of the sensor output to an external device.

57. (New) A method comprising:
activating a thermal management system of a die;
measuring a temperature on the die with a sensor of the thermal management system;
providing a first state at an output of the sensor when the temperature is below a trip point;
providing a second state at the sensor output when the temperature equals or exceeds the trip point;
engaging a power reduction mechanism in response to the sensor output having the second state;
providing the first state at the sensor output when the temperature is below an untrip point, the untrip point less than the trip point; and
halting the power reduction mechanism in response to the first state.

58. (New) The method of claim 57, further comprising engaging the power reduction mechanism to perform at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by internal clock circuitry on the die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

59. (New) The method of claim 57, further comprising providing an enable bit to a register from an external operating system to activate the thermal management system.

60. (New) The method of claim 57, further comprising:
incrementing an up-down counter coupled with the sensor output once for every clock pulse of a clock signal provided by internal clock circuitry on the die when the sensor output exhibits the first state; and
decrementing the up-down counter once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the second state.

61. (New) The method of claim 57, further comprising:
defining a plurality of trip temperatures, a highest of the plurality of trip temperatures corresponding to the trip point;
assigning a plurality of duty cycle values to the plurality of trip temperatures, one duty cycle value of the plurality of duty cycle values corresponding to at least one of the plurality of trip temperatures; and
providing a clock signal from internal clock circuitry on the die, the clock signal exhibiting the one duty cycle value in response to the temperature substantially equaling the at least one corresponding trip temperature.

62. (New) The method of claim 57, further comprising counting a number of lost clock cycles resulting from engagement of the power reduction mechanism.

63. (New) The method of claim 57, further comprising providing an indication of a status of the sensor output to an external device.